IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: PETROLLI, Jean Paul

SERIAL NO.: 10/585,696 ART UNIT: 2128

FILED: May 18, 2008 EXAMINER: Alhua S. A.

TITLE: PROGRAMMABLE LOGIC ARRAY FOR SCHEDULE-CONTROLLED PROCESSING

Amendment A: CLAIM AMENDMENTS

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (canceled)

10. (canceled)

11. (canceled)

12. (canceled)

13. (canceled)

14. (canceled)

15. (new) A data processing circuit that emulates a logic function, the data processing circuit comprising:

a single clock providing representative signals of time units;

a synchronous programmable logic array that processes values relative to the time units;

a state change detector designating events of internal values or external values:

a signal programmer cooperative with said state change detector so as to change the state or the events; and

a scheduled times processor cooperative with said logic array so as to provide representative scheduled time signals according to signals of said state change detector or by said signal programmer of the event and by the signals of said clock, said scheduled times processor adapted to determine scheduled times at time delayed by said signal programmer, the processed values from said logic array being a result of successive scheduled times initiated by the internal values or the external values of said state change detector and by successive scheduled time determination by the scheduled times processor.

16. (new) The data processing circuit of Claim 15, said logic array providing a simulator operation, the time unit being tuned for a reproduction of the simulator operation.

17. (new) The data processing circuit of Claim 15, said logic array emulating at realtime a logic function without logic emulation.

18. (new) The data processing circuit of Claim 15, said logic array having an internal logic processing cells and peripheral communication cells, the signals of said scheduled times processor controlling the operation of said logic array through at least one of said internal logic processing cells or through at least one of said peripheral communication cells.

19. (new) The data processing circuit of Claim 15, the internal logic processing cells and the peripheral communication cells exchanging data through a single group of lines on which is set an exchange per time unit, the cells generating signals relative to random events or scheduled events to said scheduled times processor, said scheduled times processor providing a command group to each of the cells.

20. (new) The data processing circuit of Claim 18, said internal logic processing cells processing a logic word per time unit.

21. (new) The data processing circuit of Claim 20, said internal logic processing cells adapted to merge several data groups issued with serval respective identities and to memorize each merged logic word.

22. (new) The data processing circuit of Claim 20, said peripheral communication cells adapted to sample the logic words received and to generate merged logic words.

23. (new) The data processing circuit of Claim 19, said logic array communicating external of the circuit, said logic array setting up memorized logic words adapted to be read or modified.